REMARKS

Claims 11 and 18 are currently amended. Applicant respectfully submits that the amendments contained herein are fully supported by the specification and drawings as originally filed and do not contain new matter.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-4, 6-8, 11, 13-15, 17-20, 22-28, and 30-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Robinson (U.S. Patent No. 5,937,423). Applicant respectfully traverses.

Claims 1, 11 (as currently amended), 14, 18 (as currently amended), and 19 each recite that an updateable register bank is adapted to send a first signal to an analog/memory core of a memory device for controlling operation of the analog/memory core, that a bus controller is coupled to the register bank, that the bus controller is adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank, that the first signal is sent from the register bank to the analog/memory core without passing through the bus controller, and that the bus controller is coupled between an array of flash memory cells of the memory device and a command user interface of the memory device. Applicant respectfully submits that this is different than Robinson.

The Examiner has taken registers 32-58 of Figure 3 of Robinson, i.e., command register 32, status register 33, source address register 34, destination address register 35, length register 36, erase queue register 37, and data I/O registers 38-58, as corresponding to the updateable register bank of each of claims 1, 11, 14, 18, and 19. The Examiner has taken blocks of flash EEPROM memory cells 68 as corresponding the analog/memory core of each of claims 1, 11, 14, 18, and 19 and an I/O data signal from data I/O registers 38-58 as corresponding to the first signal of each of claims 1, 11, 14, 18, and 19. However, Applicant contends that the I/O data is merely stored in the blocks of flash EEPROM memory cells 68 and does not control the operation of the blocks of flash EEPROM memory cells 68, as is required by each of claims 1, 11, 14, 18, and 19. Control of the operation of the analog/memory core of each of claims 1, 11, 14, 18, and 19 is at least discussed in paragraph [0024] of the specification of the present application. For example, paragraph [0024] indicates that control of the operation of the analog/memory core may include causing programming voltages, soft-programming voltages, program-verify voltages to be applied to memory cells of the memory array of each of claims 1,

11, 14, 18, and 19 or causing the analog/memory core to execute an erase, a compaction, a program-verify, etc. Applicant contends that an I/O data signal from data I/O registers 38-58 does not control the operation of the blocks of flash EEPROM memory cells 68 as that term is used and recited in each of claims 1, 11, 14, 18, and 19.

The Examiner has taken address decode circuitry 63, command decode circuit 60, high voltage circuitry 61, and state machines 64 of Figure 3 of Robinson as collectively corresponding to the bus controller of each of claims 1, 11, 14, 18, and 19, and command register 32 as corresponding to the command user interface of each of claims 1, 11, 14, 18, and 19. However, as indicated above, the Examiner has already taken command register 32 as corresponding to the register bank of each of claims 1, 11, 14, 18, and 19. That is, the Examiner has taken command register 32 to correspond to two inconsistent elements of each of claims 1, 11, 14, 18, and 19, which is improper, i.e., the first signal cannot be sent from the register bank without passing through the bus controller if the register bank and the bus controller are not mutually exclusive.

The Examiner has taken a signal from any one of registers 33-37 as corresponding to the second signal of each of claims 1, 11, 14, 18, and 19. However, Figure 3 of Robinson shows that signals from registers 33-37 are sent to a data multiplexer 62 and not to any of address decode circuitry 63, command decode circuit 60, high voltage circuitry 61, and state machines 64, taken to correspond to the bus controller of each of claims 1, 11, 14, 18, and 19 by the Examiner. The Examiner has taken the signal from address decode circuitry 63 to register select 59 as corresponding to the third signal of each of claims 1, 11, 14, 18, and 19. However, there is no suggestion or indication in Robinson that this signal updates registers 32-58, as specified by each of claims 1, 11, 14, 18, and 19. Applicant submits that updating the register bank of each of claims 1, 11, 14, 18, and 19 means to change the contents of the register bank (see paragraph [0033] of the present application). The Examiner indicates that the signal from address decode circuitry 63 to register select 59 selects a specific register of registers 32-58. Applicant contends that selects a specific register of registers 32-58 does not necessarily mean updating (or changing the contents) of a specific register of registers 32-58.

In view of the above, Applicant respectfully submits that Robinson does not include each and every recitation of each of claims 1, 11, 14, 18, and 19. Therefore, each of claims 1, 11, 14, 18, and 19 should be allowed.

Claims 2-4 and 6-8 depend from claim 1 and are thus allowable for at least the same reasons as claim 1. Claim 13 depends from claim 11 and is thus allowable for at least the same reasons as claim 11. Claims 15 and 17 depend from claim 14 and are thus allowable for at least the same reasons as claim 14. Claims 20 and 22-23 depend from claim 19 and are thus allowable for at least the same reasons as claim 19.

Claim 24 recites: "receiving first data at a bus controller of the memory device controller from a first register of a register bank of the memory device controller; sending second data from the bus controller to the first or a second register of the register bank for updating the register bank; and sending a control signal from a third register of the register bank to an analog/memory core of the memory device for controlling operation of the analog/memory core, the analog/memory core comprising an array of flash memory cells and supporting analog access circuitry; wherein the control signal is sent from the third register of the register bank to the analog/memory core without passing through the bus controller; and wherein the bus controller is coupled between the array of flash memory cells and a command user interface of the memory device." Applicant respectfully submits that this is different than Robinson.

In the rejection of claim 24 the Examiner refers to the reasons given for claim 1. Applicant takes this to mean that the Examiner has taken registers 32-58, i.e., command register 32, status register 33, source address register 34, destination address register 35, length register 36, erase queue register 37, and data I/O registers 38-58, as corresponding to the register bank of claim 24, blocks of flash EEPROM memory cells 68 as corresponding to the analog/memory core of claim 24, address decode circuitry 63, command decode circuit 60, high voltage circuitry 61, and state machines 64 as collectively corresponding to the bus controller of claim 24, and command register 32 as corresponding to the command user interface of claim 24. The Examiner has taken command register 32 to correspond to two different elements of claim 24, i.e., the updateable register bank of claim 24 and the command user interface of claim 24, which is improper.

Applicant contends that Robinson does not send a control signal for controlling operation of the blocks of flash EEPROM memory cells 68 from any register of registers 32-58 to the blocks of flash EEPROM memory cells 68 without passing through address decode circuitry 63, command decode circuit 60, high voltage circuitry 61, and state machines 64. Instead, Robinson sends an I/O data signal from data I/O registers 38-58 to the blocks of flash EEPROM memory cells 68 without passing through address decode circuitry 63, command decode circuit 60, high

voltage circuitry 61, and state machines 64. However, an I/O data signal from data I/O registers 38-58 is different than a control signal for controlling operation of the blocks of flash EEPROM memory cells 68. Indeed, the I/O data signal from data I/O registers 38-58 does not control operation of the blocks of flash EEPROM memory cells 68 in the same sense indicated by claim 24 and at least discussed in paragraph [0024] of the specification of the present application. Also, as indicated above in conjunction with each of claims 1, 11, 14, 18, and 19, there is no indication in Robinson of a signal from address decode circuitry 63, command decode circuit 60, high voltage circuitry 61, and state machines 64 (taken to be the bus controller of claim 24 by the Examiner) for updating any of registers 32-58.

In view of the above, Applicant respectfully submits that Robinson does not include each and every recitation of claim 24. Therefore, claim 24 should be allowed.

Claims 25-28 and 30-31 depend from claim 24 and are thus allowable for at least the same reasons as claim 24.

Claim Rejections Under 35 U.S.C. § 103

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Robinson (U.S. Patent No. 5,937,423). Applicant respectfully traverses.

The taking of Official Notice that Robinson implies that a series of clocks are used to facilitate operations and that the exact number of clocks lacks patentable significance fails to overcome the deficiencies of Robinson with regard to claim 1. Claim 5 depends from claim 1 and is thus allowable for at least the same reasons as claim 1.

Claims 9, 12, 16, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Robinson (U.S. Patent No. 5,937,423) and in view of Ratcliff (U.S. Patent No. 4,797,876). Applicant respectfully traverses.

Claims 1, 11 (as currently amended), 14, and 19 are each patentably distinct from Robinson. Robinson in combination with Radcliff fails to overcome the deficiencies of Robinson with respect to each of claims 1, 11, 14, and 19. Therefore, claims 1, 11, 14, and 19 are allowable over Robinson in view of Radcliff. Claim 9 depends from claim 1 and is thus allowable for at least the same reasons as claim 1. Claim 12 depends from claim 11 and is thus allowable for at least the same reasons as claim 11. Claim 16 depends from claim 14 and is thus

allowable for at least the same reasons as claim 14. Claim 21 depends from claim 19 and is thus allowable for at least the same reasons as claim 19.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2208.

Respectfully submitted,

Date: 03-19-07

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